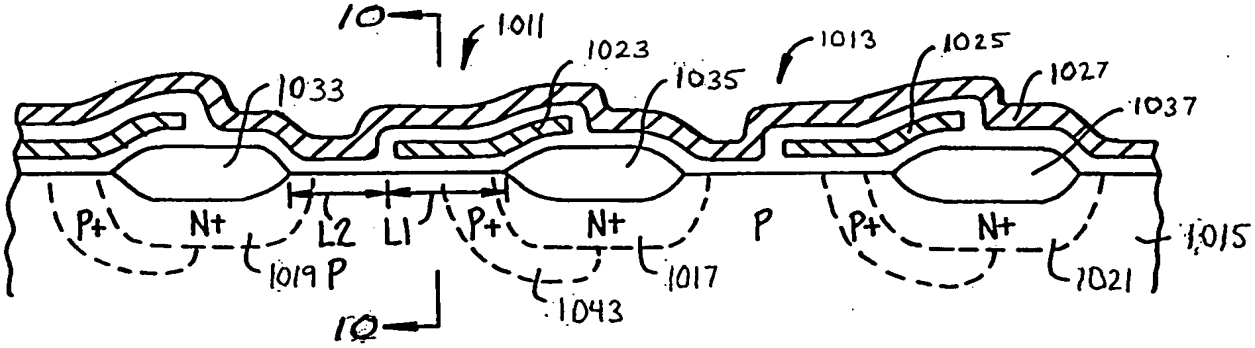


FIG. 9

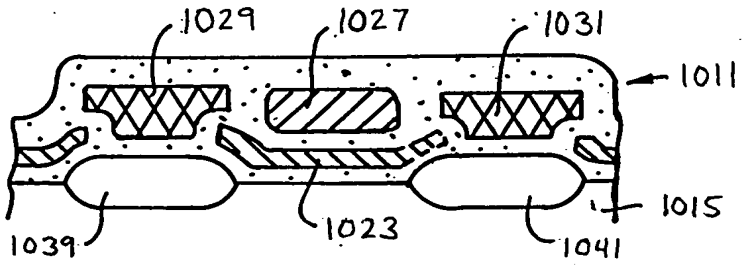


FIG. 10

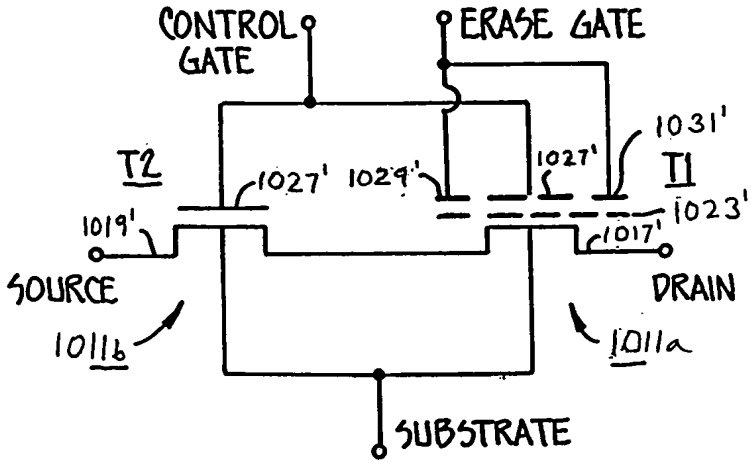


FIG. 11

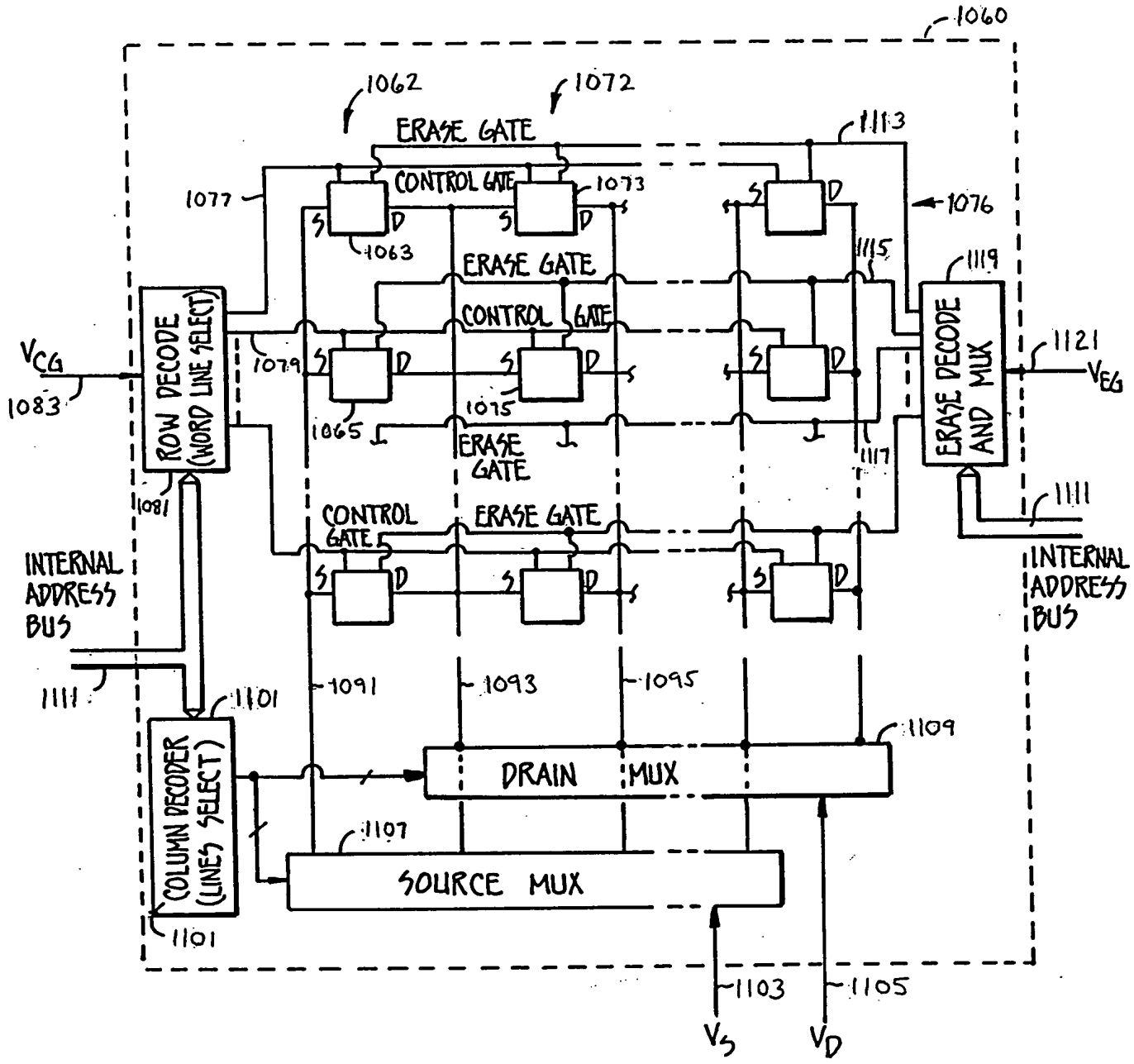

1060
1062
1072
ERASE GATE
1113
CONTROL GATE
1073
1077
1076
1063
ERASE GATE
1115
1119
CONTROL GATE
ROW DECODE (WORD LINE SELECT)
ERASE DECODE AND MUX
1121
V_{EG}
V_{CG}
1083
1079
1075
1065
ERASE GATE
1117
1081
CONTROL GATE
ERASE GATE
1111
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
1111
1101
1091
1093
1095
1109
DRAIN MUX
1107
SOURCE MUX
COLUMN DECODER (LINES SELECT)
1101
1103
1105
V_S
V_D

FIG. 12.

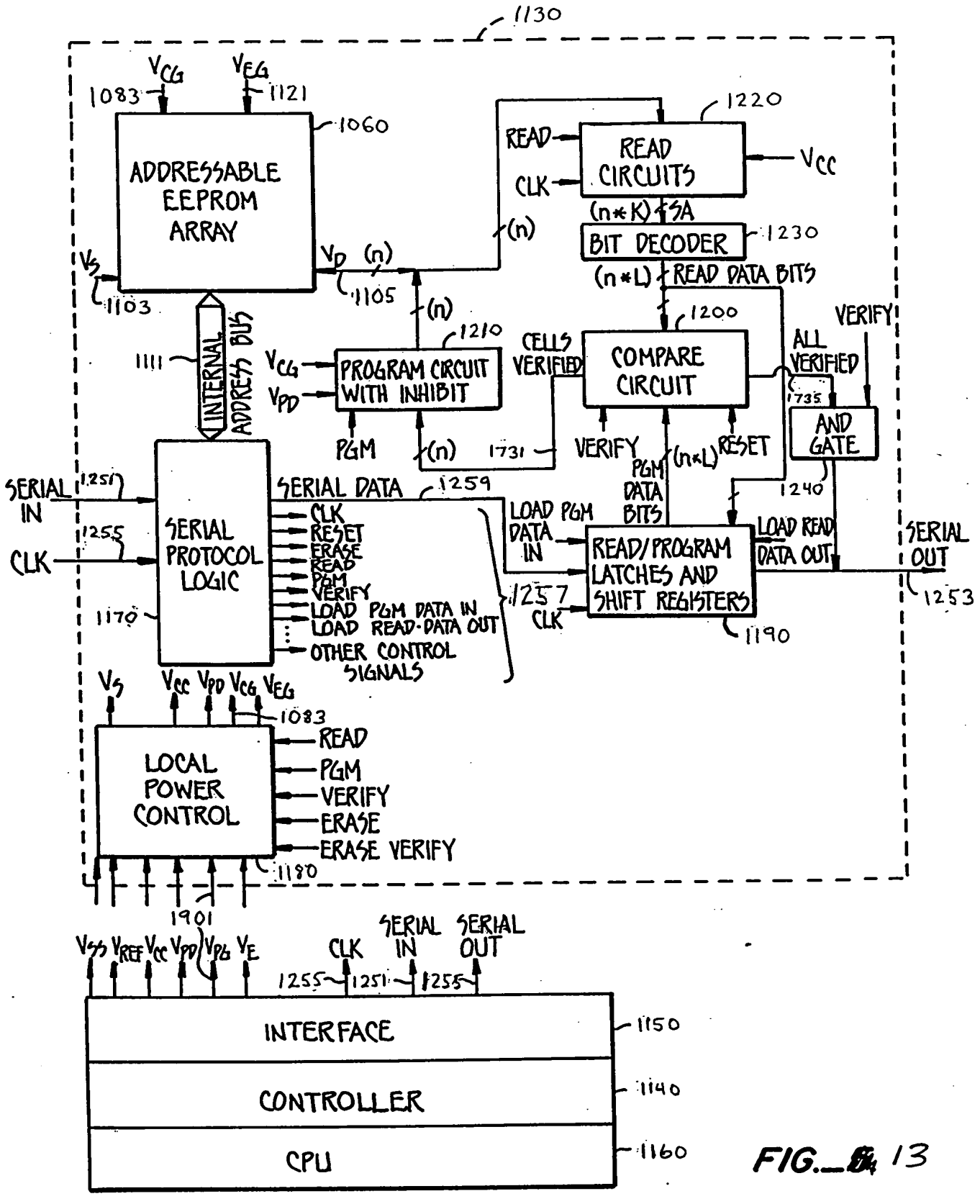

1130
V_{CG}
V_{EG}
1083
1121
1060
ADDRESSABLE EEPROM ARRAY
V_S
1103
V_D (n)
1105
1111
INTERNAL ADDRESS BUS
1220
READ
CLK
READ CIRCUITS
V_{CC}
(n*K) SA
1230
BIT DECODER
(n*L) READ DATA BITS
(n)
1210
V_{CG}
V_{PD}
PROGRAM CIRCUIT WITH INHIBIT
PGM
(n)
1731
1200
CELLS VERIFIED
COMPARE CIRCUIT
ALL VERIFIED
1735
VERIFY
AND GATE
1240
VERIFY
PGM DATA BITS
(n*L)
RESET
SERIAL IN
1251
SERIAL PROTOCOL LOGIC
1255
CLK
1170
SERIAL DATA
1259
CLK
RESET
ERASE
READ
PGM
VERIFY
LOAD PGM DATA IN
LOAD READ-DATA OUT
OTHER CONTROL SIGNALS
LOAD PGM DATA IN
1257
CLK
READ/PROGRAM LATCHES AND SHIFT REGISTERS
1190
LOAD READ DATA OUT
SERIAL OUT
1253
V_S
V_{CC}
V_{PD}
V_{CG}
V_{EG}
1083
LOCAL POWER CONTROL
READ
PGM
VERIFY
ERASE
ERASE VERIFY
1180
1901
V_{SS}
V_{REF}
V_{CC}
V_{PD}
V_{PG}
V_E
CLK
SERIAL IN
SERIAL OUT
1255
1251
1255
INTERFACE
1150
CONTROLLER
1140
CPU
1160

FIG. 13

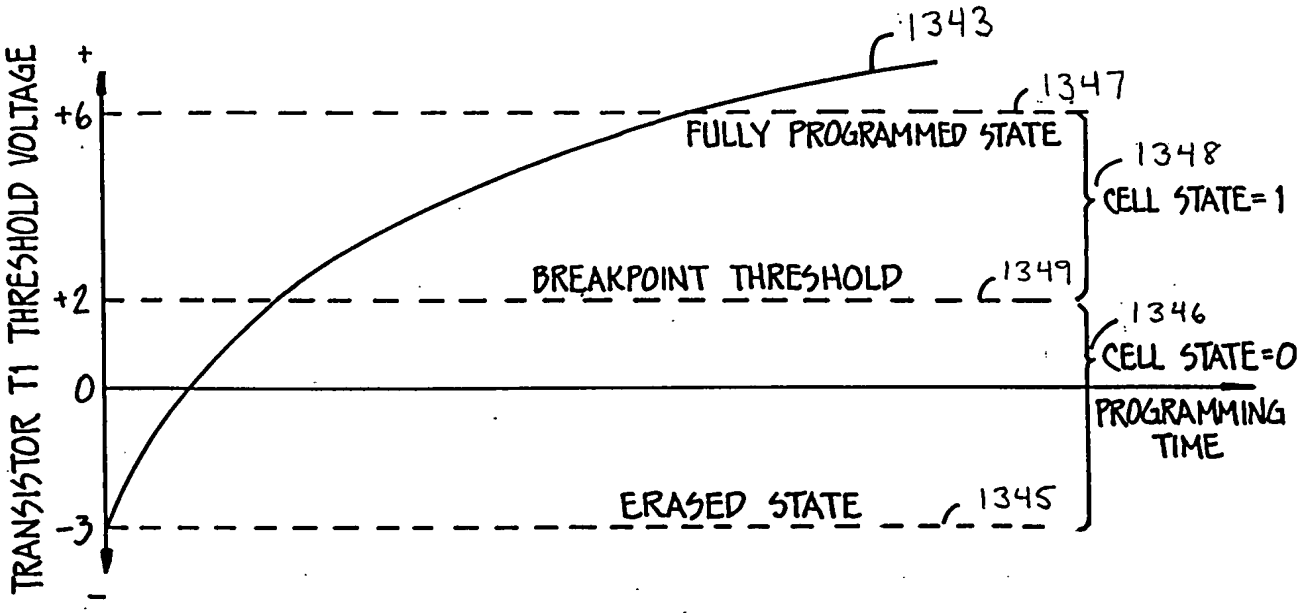


FIG. 14.

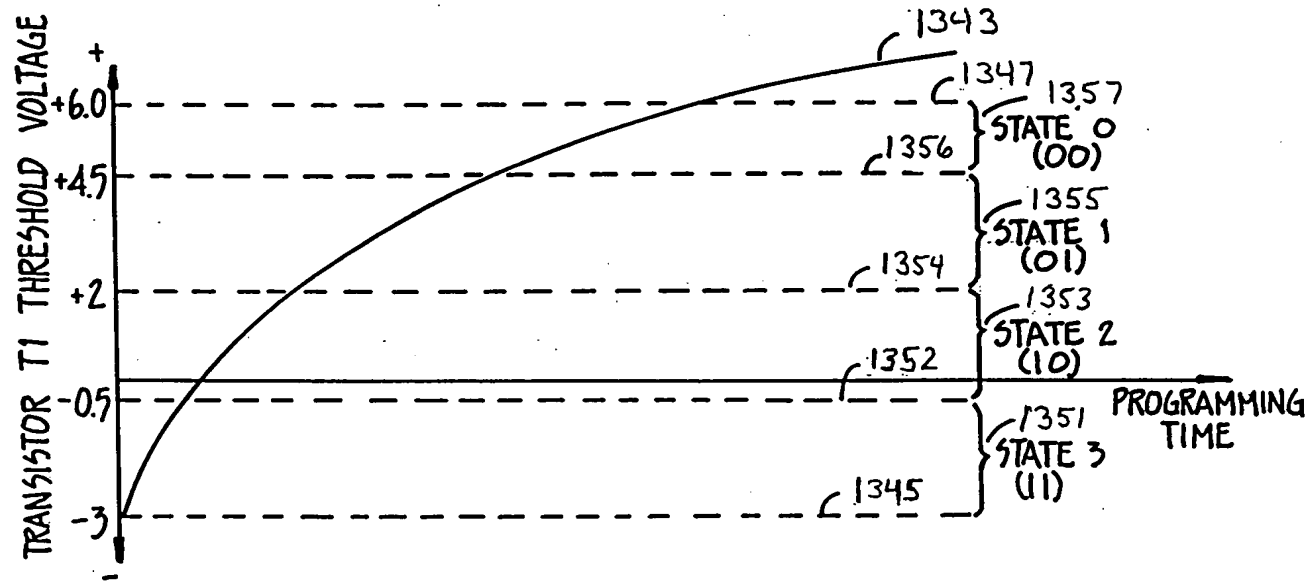


FIG. 15A

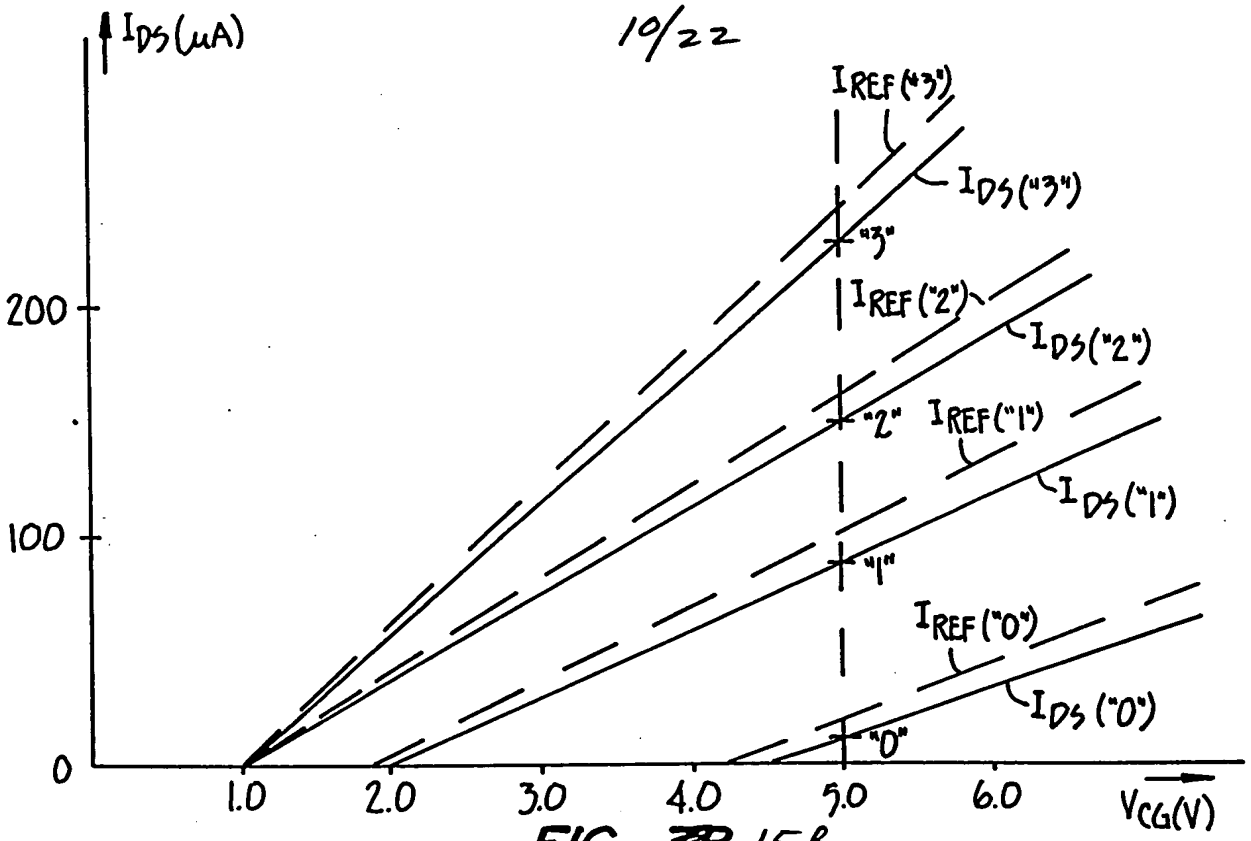


FIG. 15B

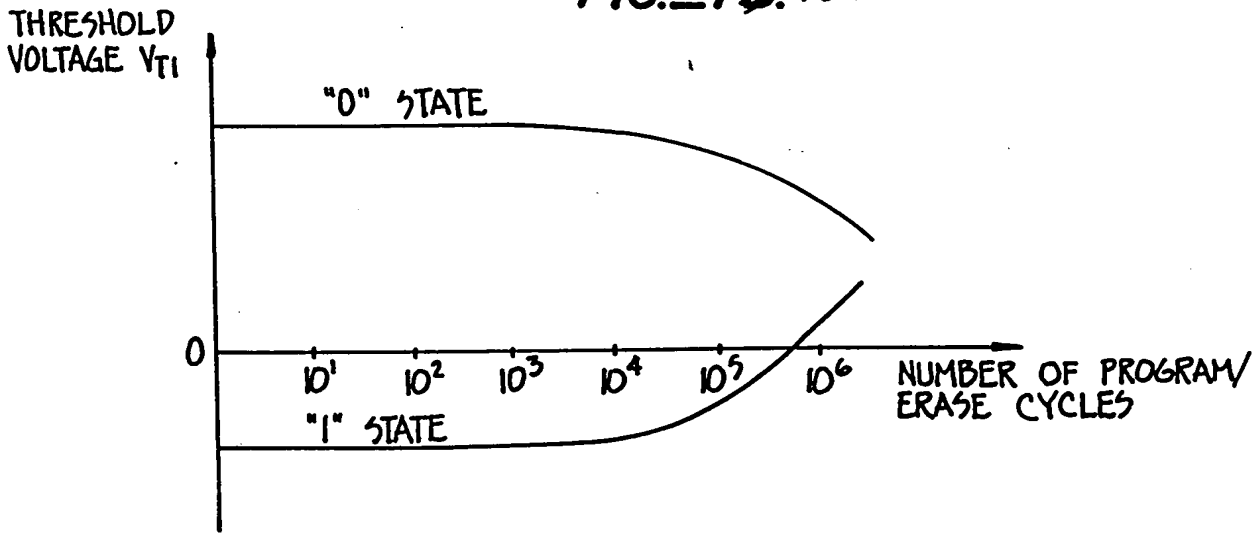


FIG. 16A

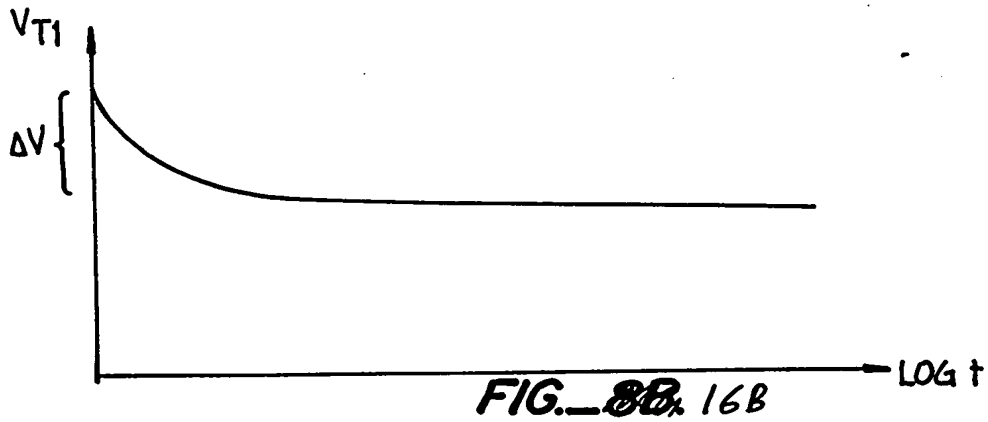


FIG. 16B

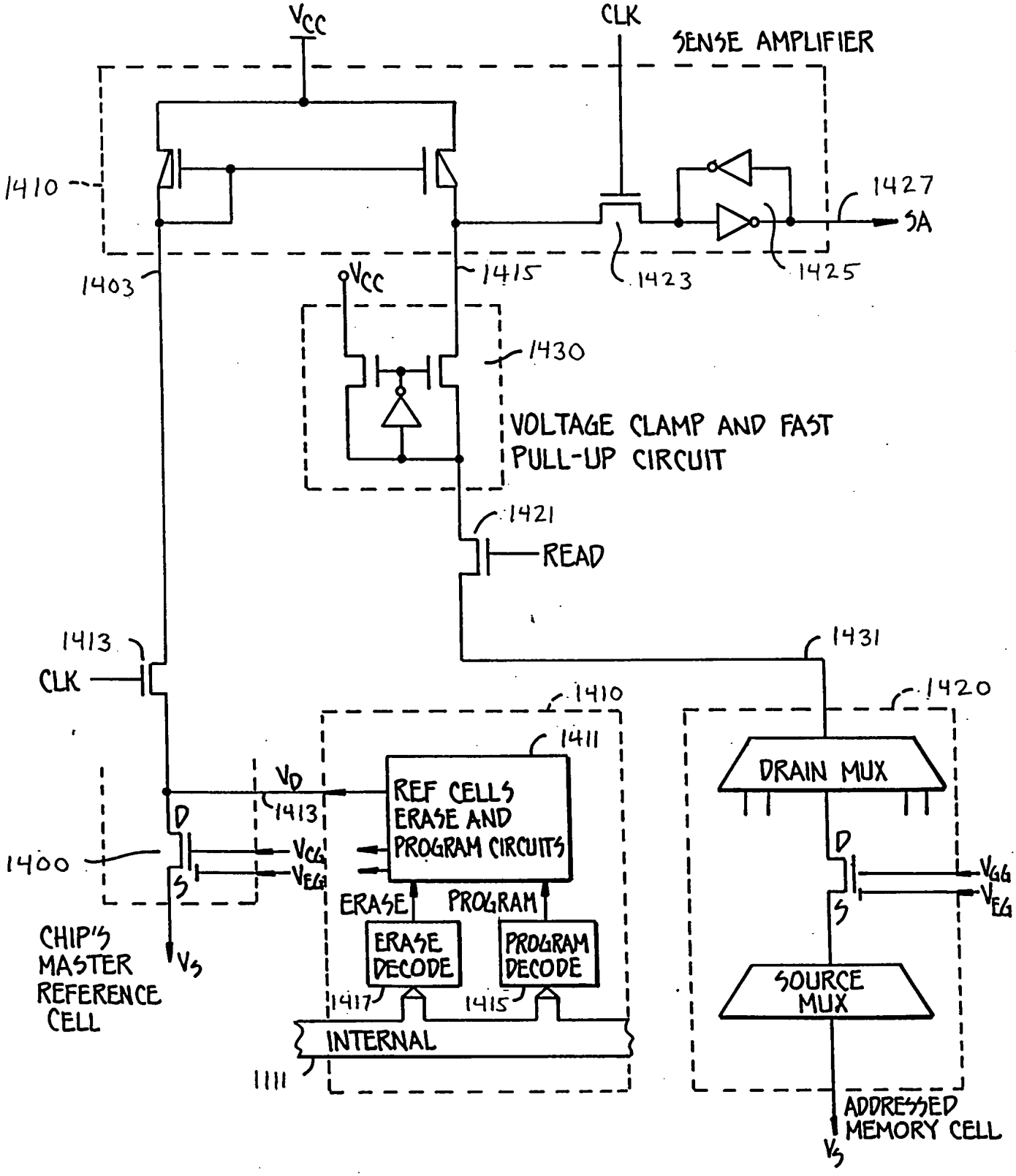

V_{CC}
CLK
SENSE AMPLIFIER
1410
1427
SA
1403
1415
1423
1425
V_{CC}
1430
VOLTAGE CLAMP AND FAST PULL-UP CIRCUIT
1421
READ
1413
CLK
1431
1410
1420
1411
V_D
1413
REF CELLS ERASE AND PROGRAM CIRCUITS
DRAIN MUX
D
1400
V_{CG}
V_{EG}
S
ERASE
PROGRAM
V_{GG}
V_{EG}
CHIP'S MASTER REFERENCE CELL
V_S
ERASE DECODE
PROGRAM DECODE
SOURCE MUX
1417
1415
INTERNAL
1111
ADDRESSED MEMORY CELL
V_S

FIG. 8A. 17A

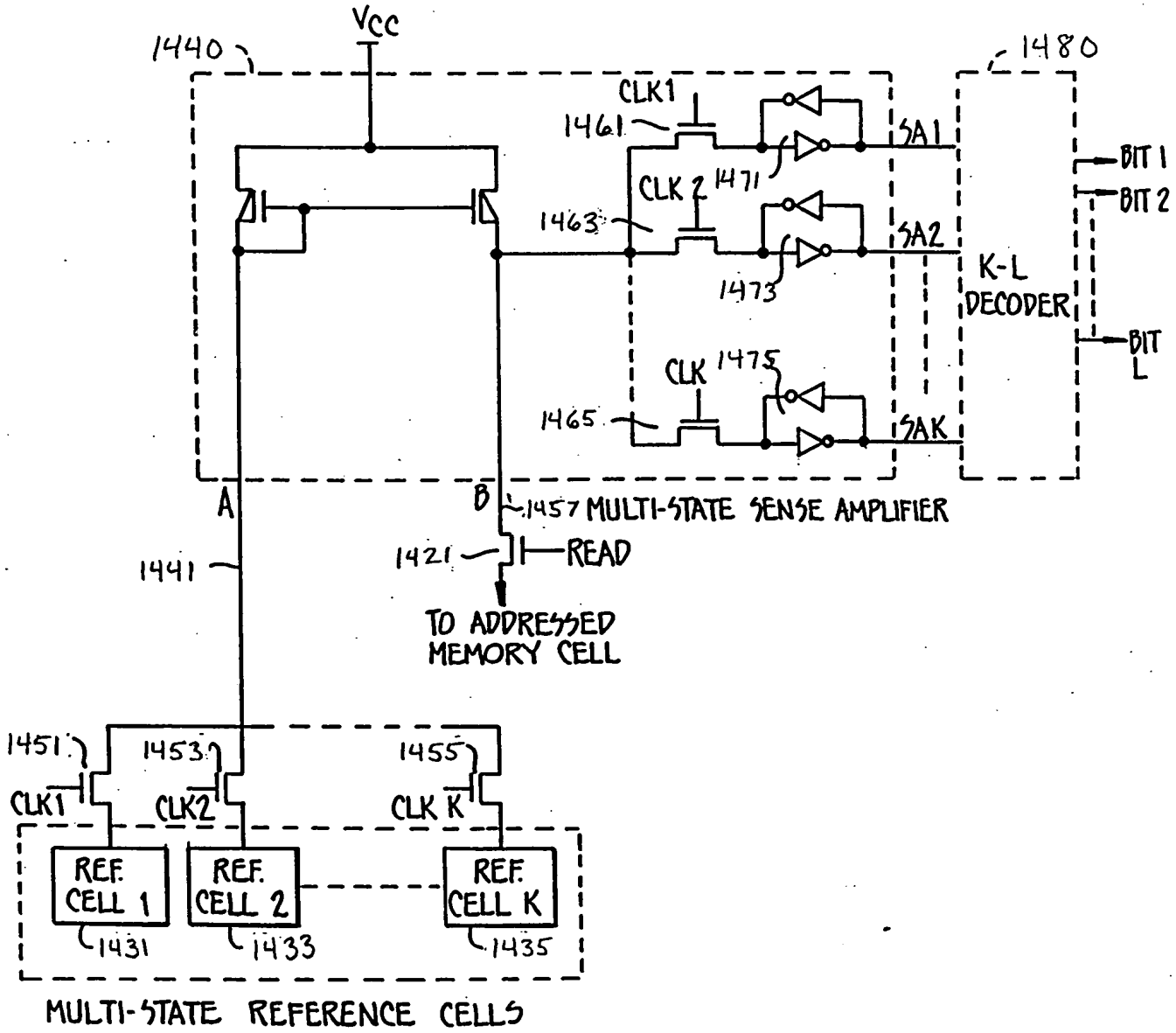

Vcc
1440
1480
CLK1
1461
SA1
BIT 1
CLK 2
1471
1463
SA2
BIT 2
K-L
DECODER
1473
CLK
1475
1465
SAK
BIT
L
A
B
1457 MULTI-STATE SENSE AMPLIFIER
1441
1421
READ
TO ADDRESSED
MEMORY CELL
1451
1453
1455
CLK1
CLK2
CLK K
REF.
CELL 1
REF.
CELL 2
REF.
CELL K
1431
1433
1435
MULTI-STATE REFERENCE CELLS

FIG. 17B

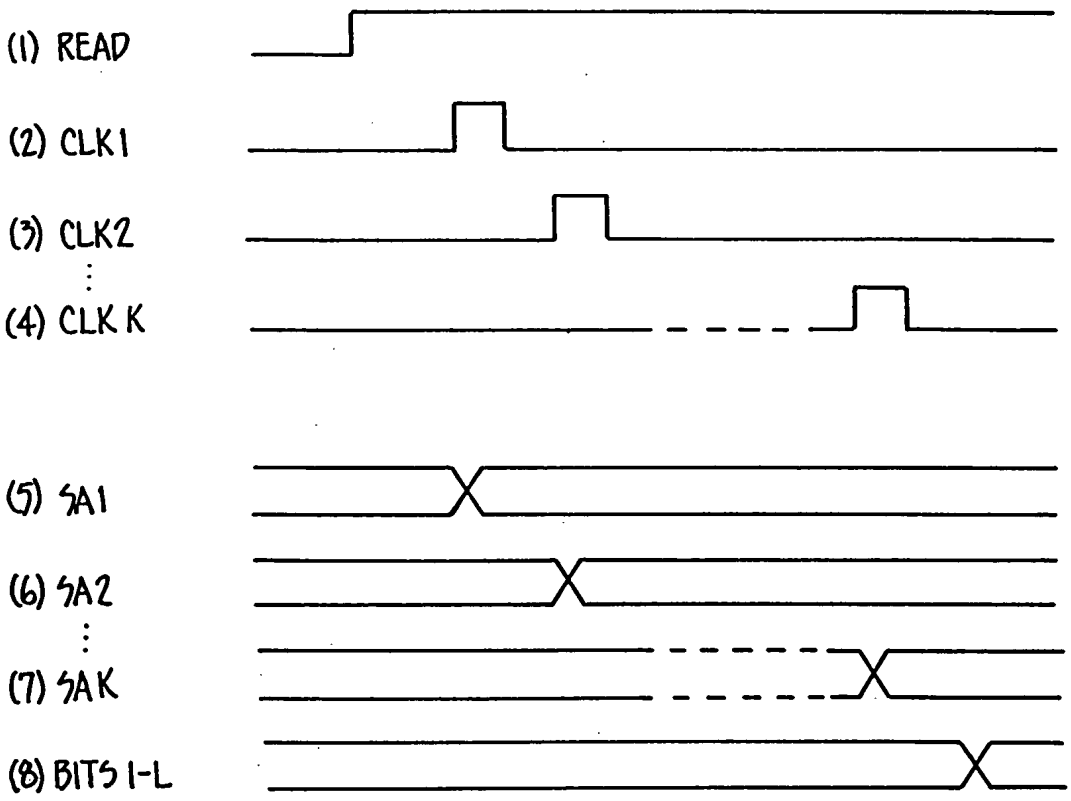


FIG. 17C

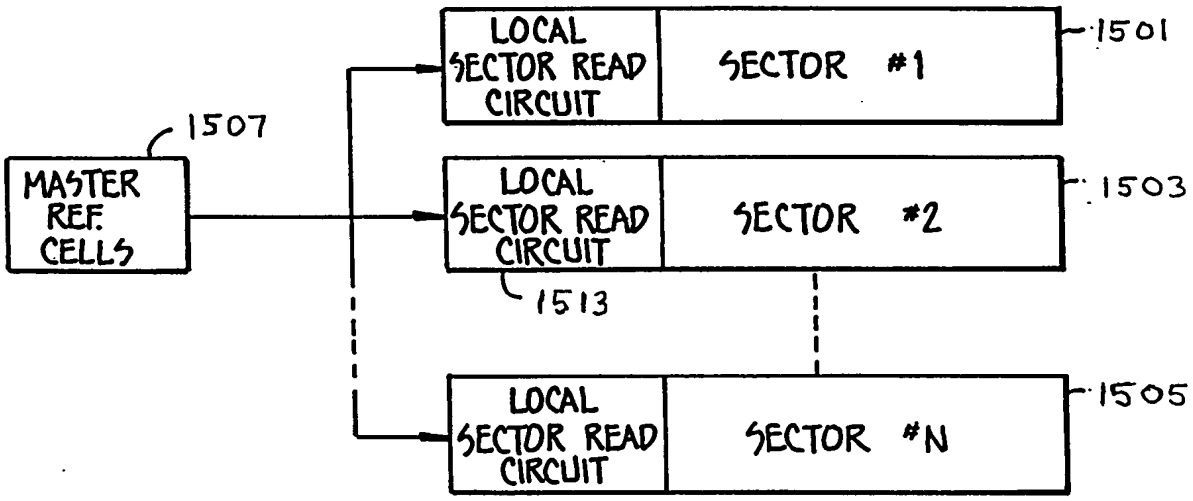


FIG. 18

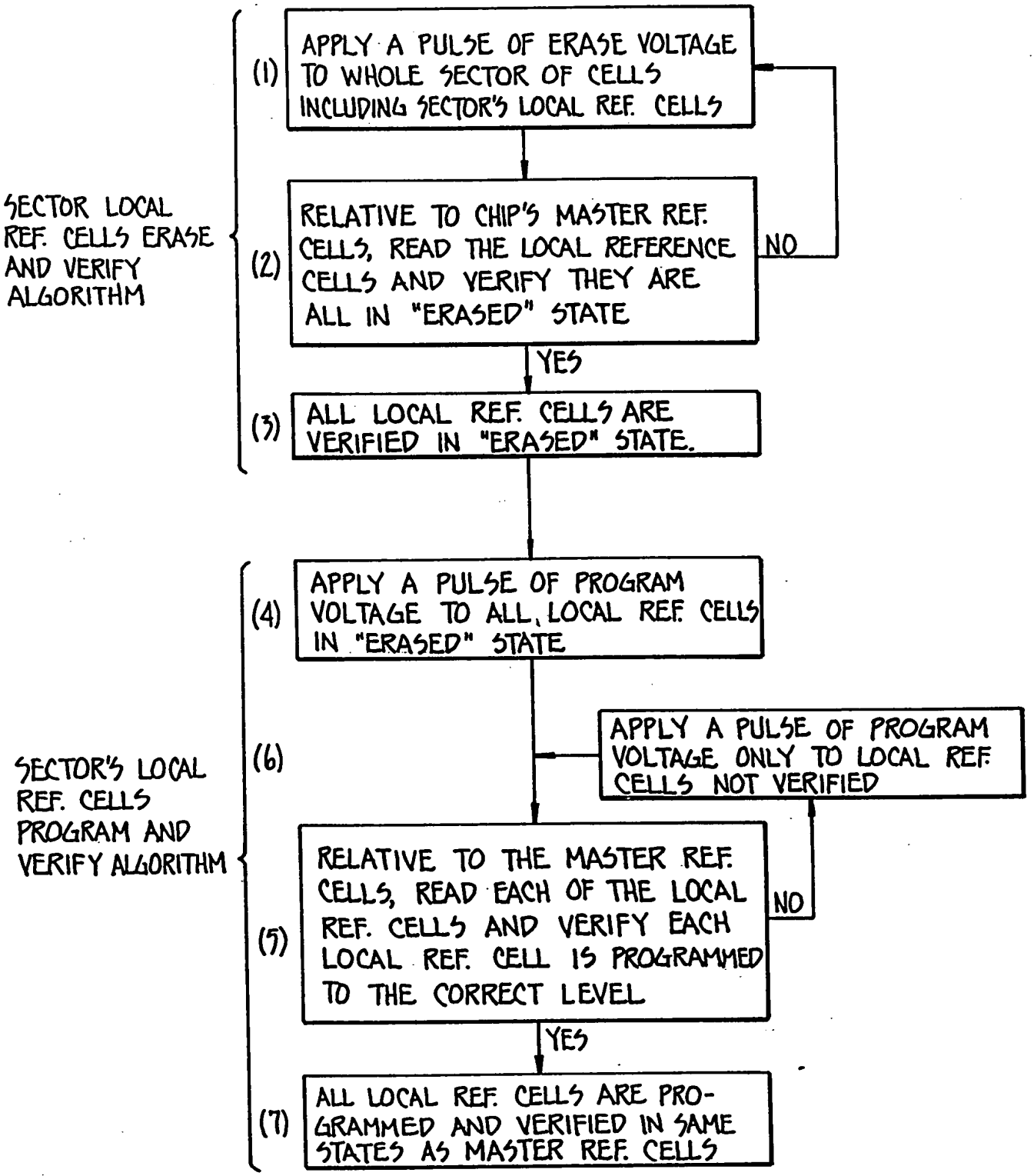


FIG. 19

Doc No. 5,963,465

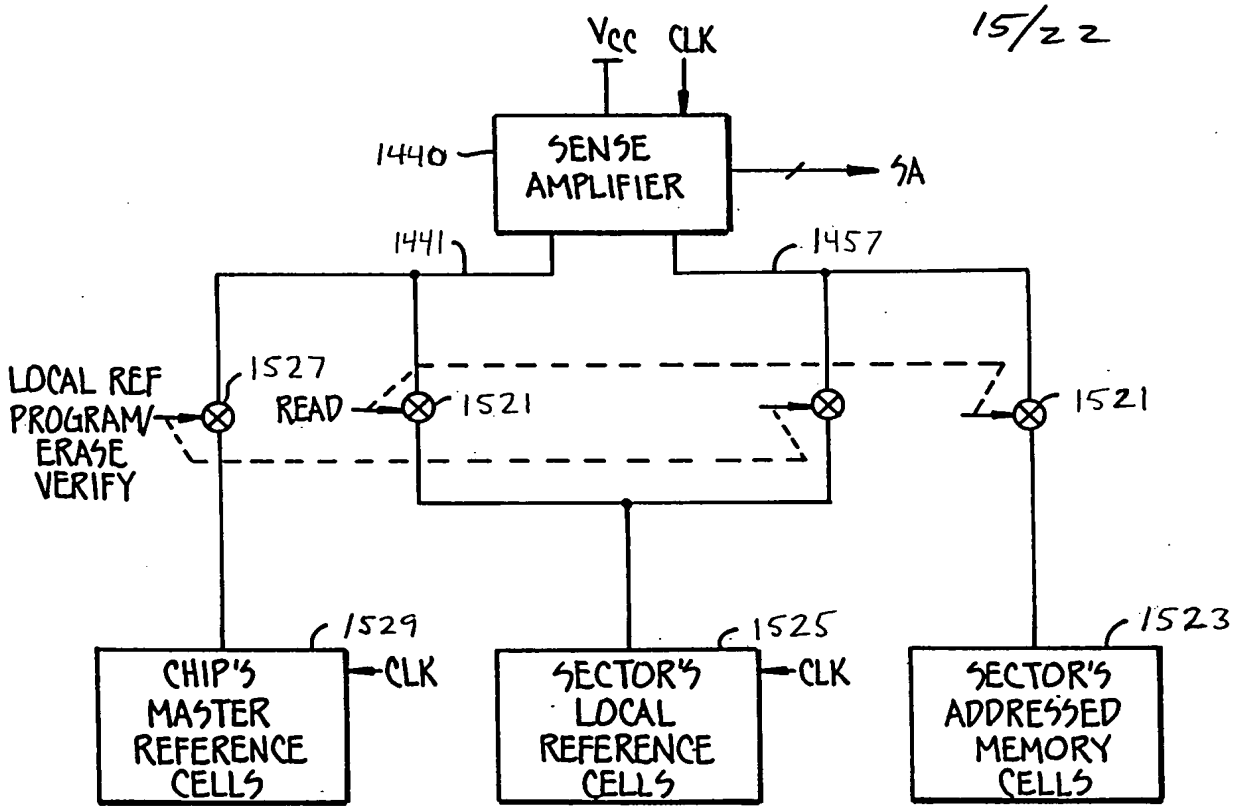


FIG. ~~12A~~ 20A

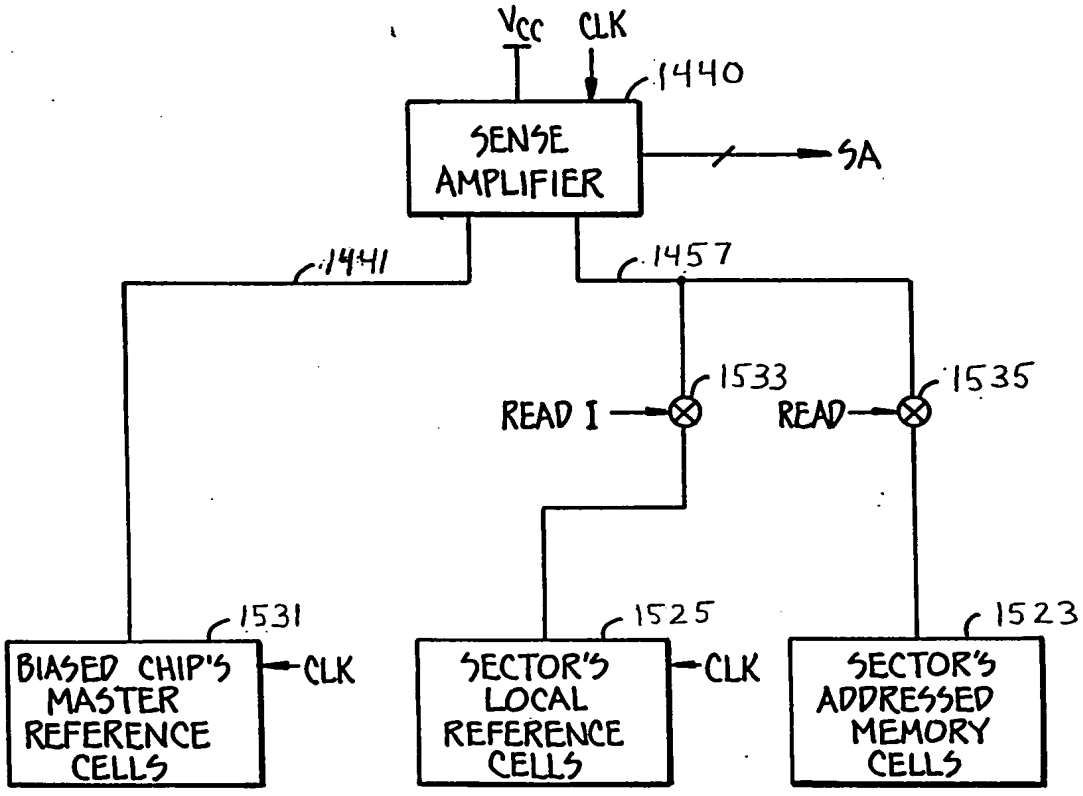


FIG. ~~13A~~ 21A

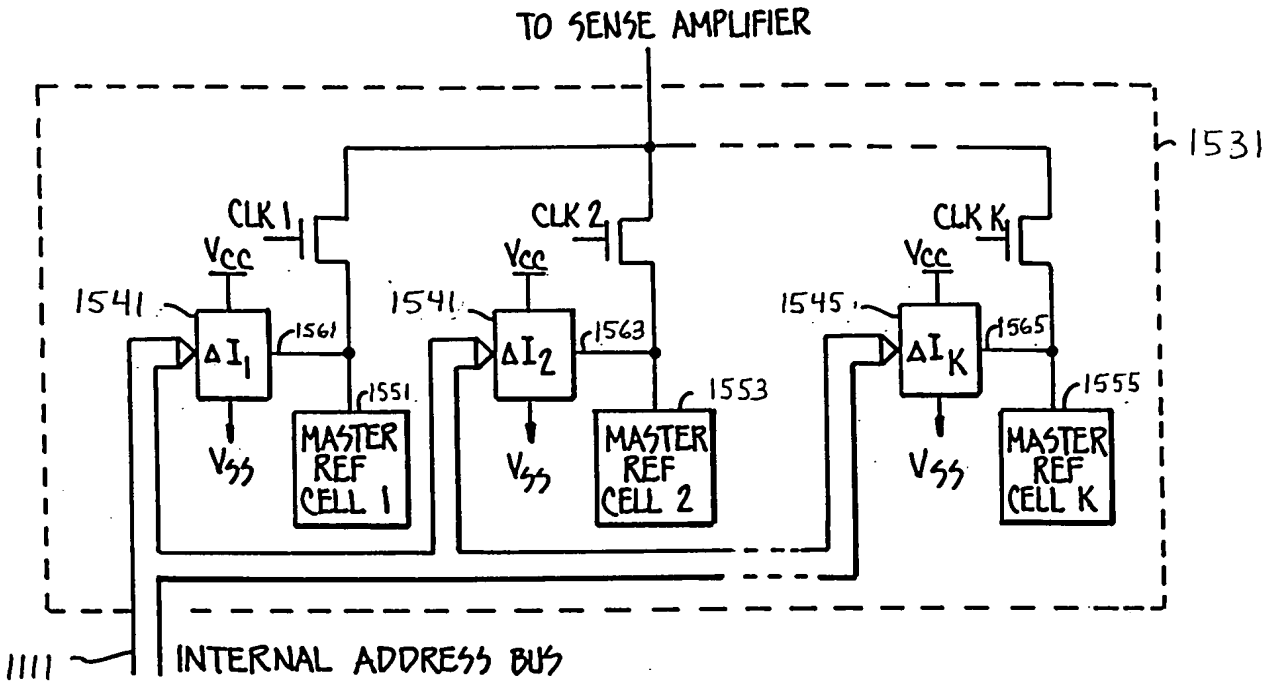


FIG. 21B

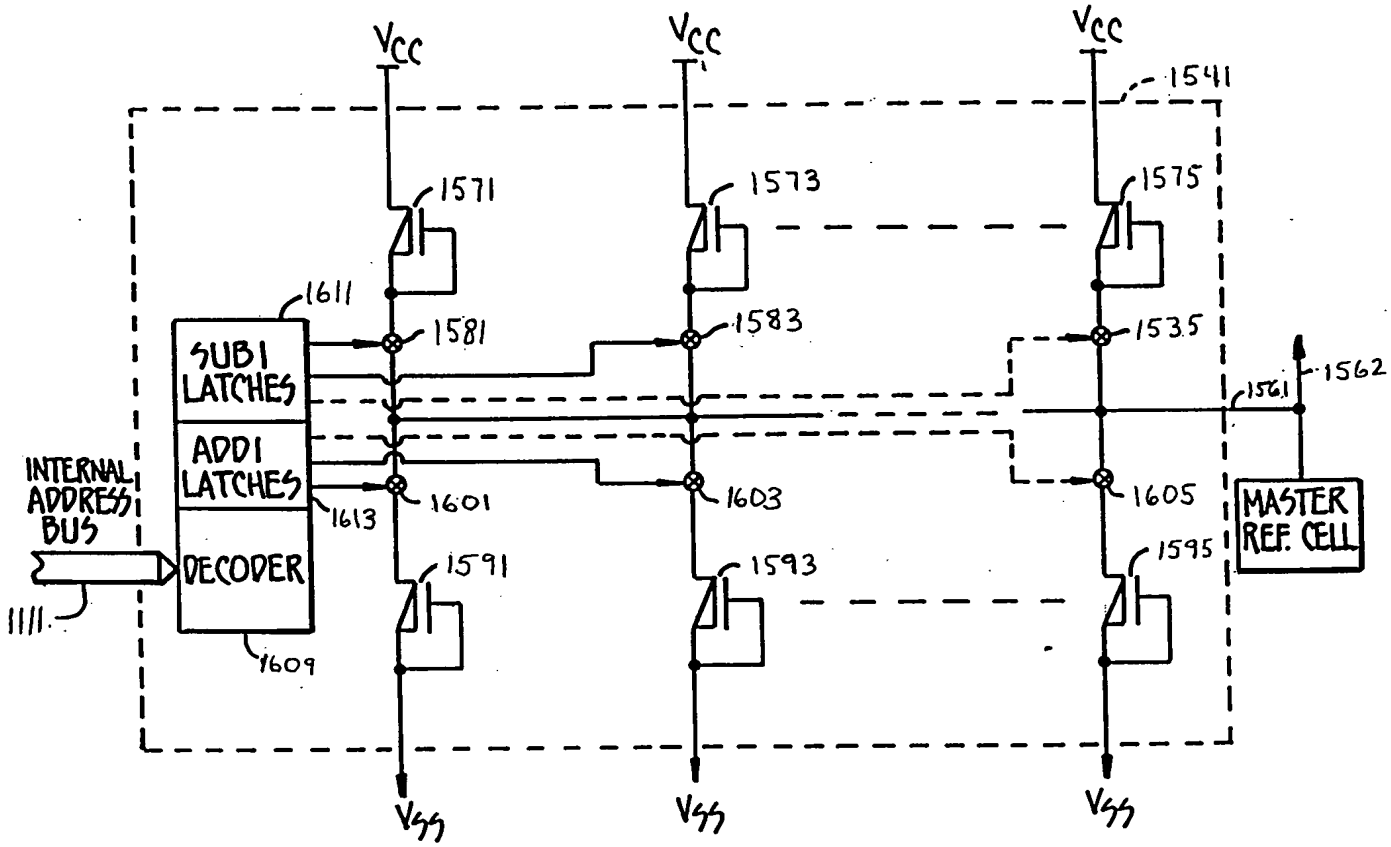


FIG. 21C

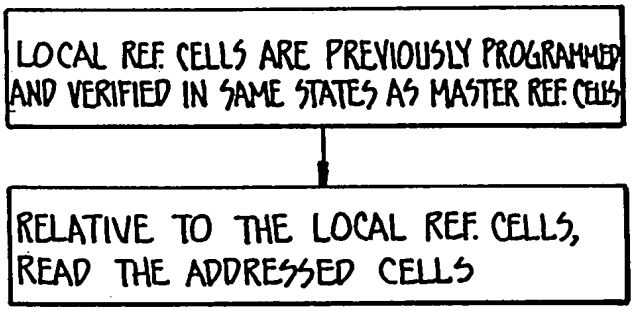


FIG. ~~12B~~, 20B

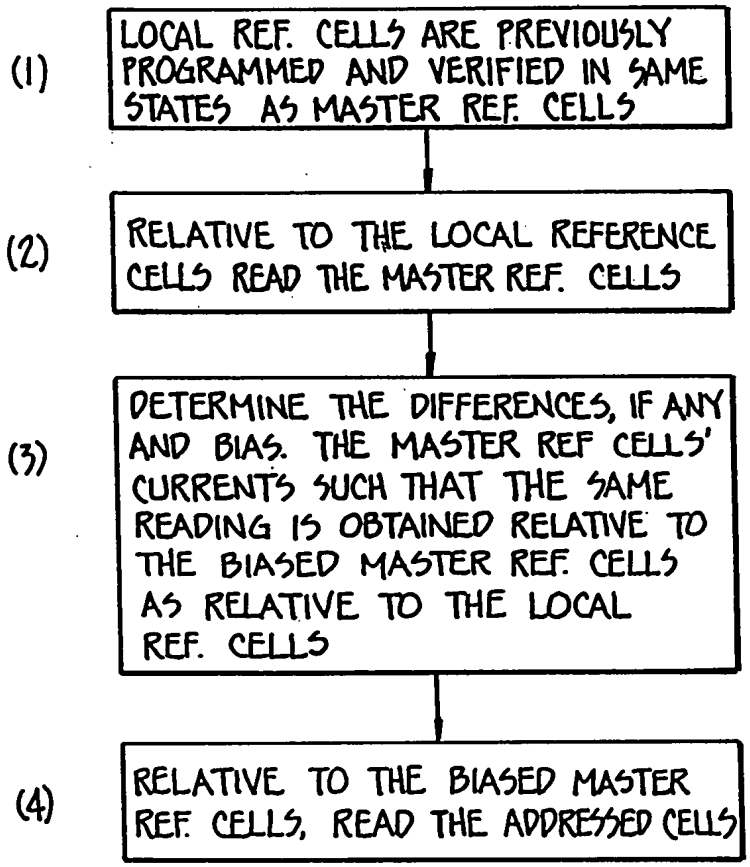
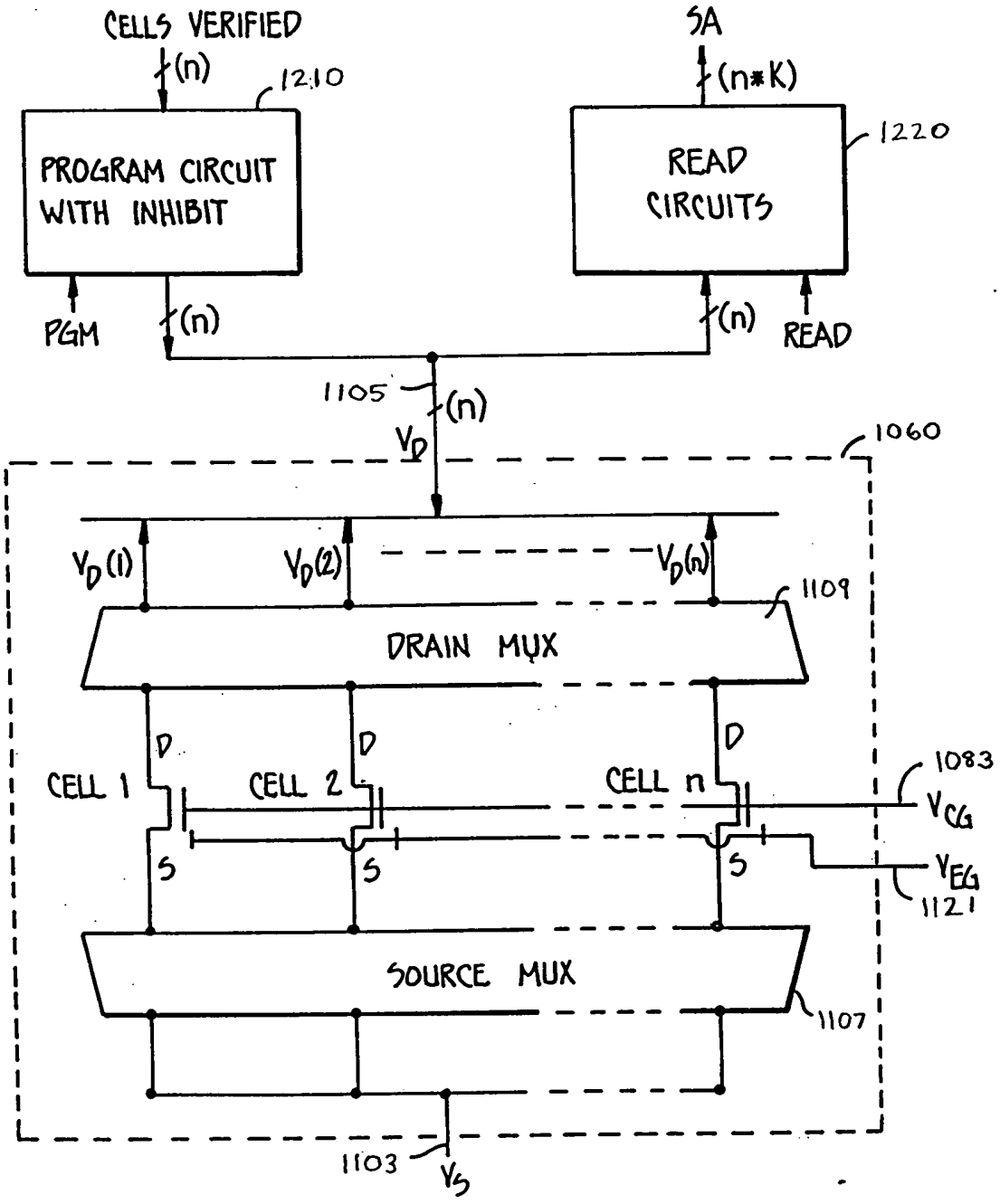


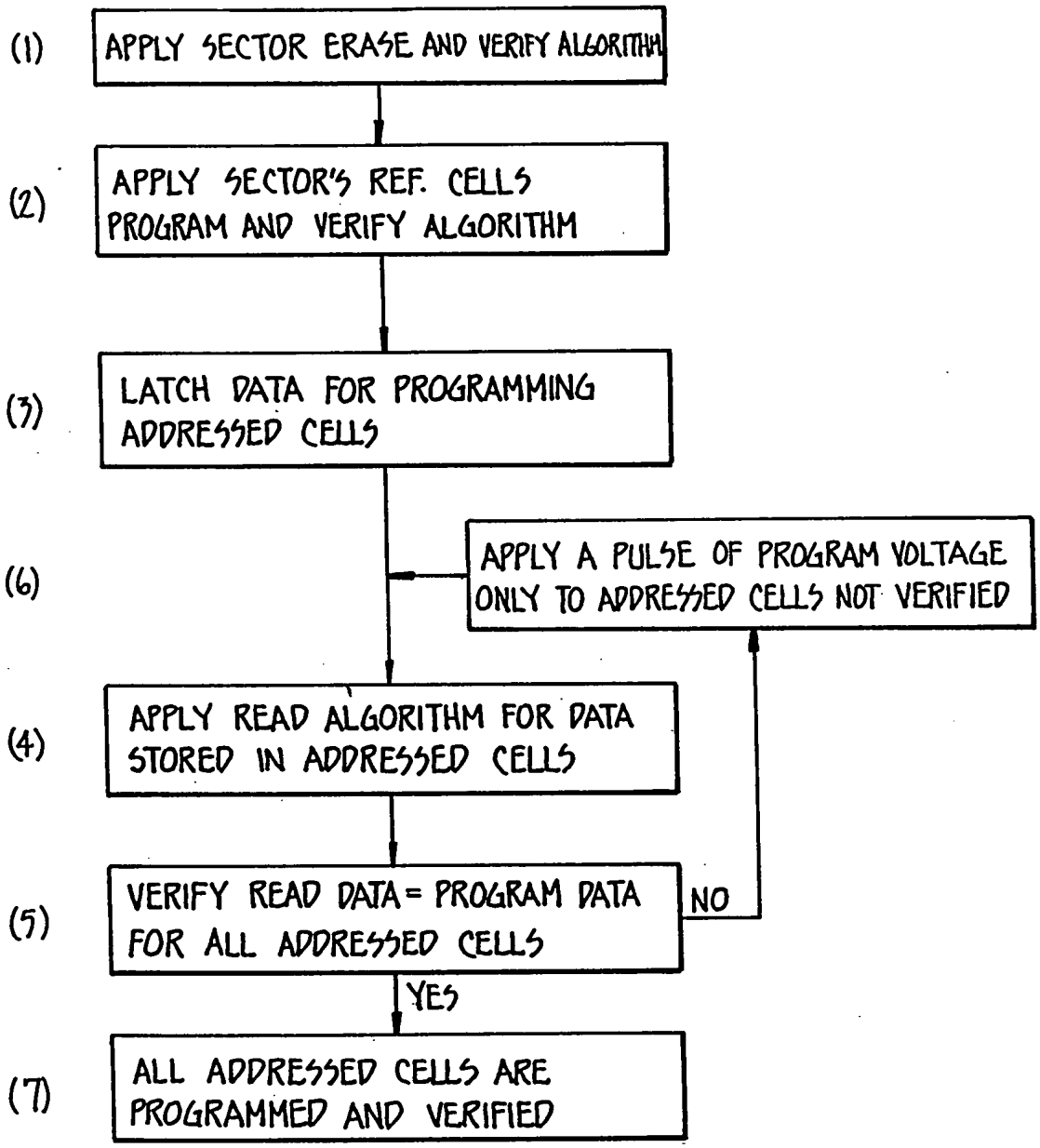
FIG. ~~13D~~, 21D

05601-1-US-00-1-98



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG. 22.



PROGRAM ALGORITHM

FIG. 15. 23

0 6 8 8 6 4 0 - 1 - 0 5 - 9 8

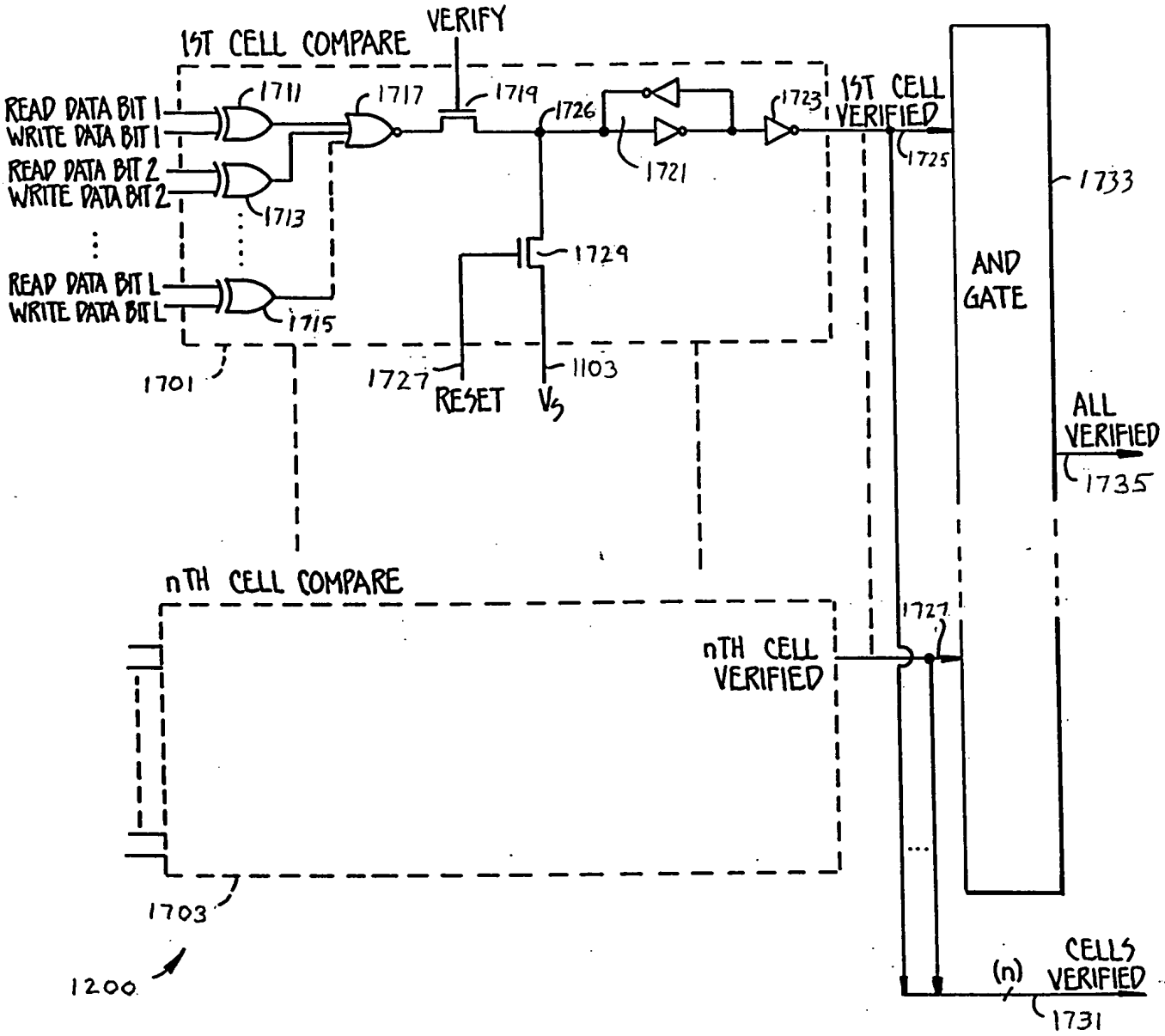

1ST CELL COMPARE
VERIFY
READ DATA BIT 1
WRITE DATA BIT 1
READ DATA BIT 2
WRITE DATA BIT 2
READ DATA BIT L
WRITE DATA BIT L
1711
1717
1719
1726
1723
1721
1713
1715
1729
1701
1727
RESET
1103
1ST CELL VERIFIED
1725
1733
AND GATE
ALL VERIFIED
1735
nTH CELL COMPARE
nTH CELL VERIFIED
1727
1703
1200
CELLS (n) VERIFIED
1731

FIG. 16. 24

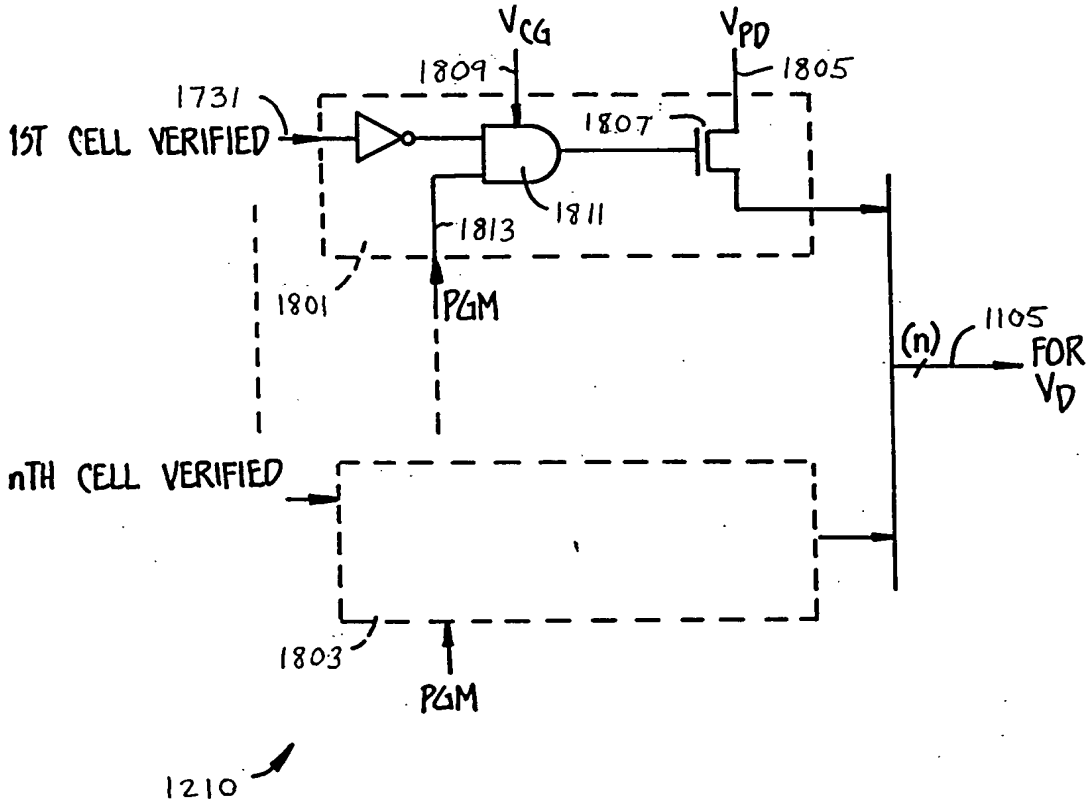

V_{CG}
V_{PD}
1809
1805
1731
1ST CELL VERIFIED
1807
1811
1813
1801
PGM
(n)
1105
FOR V_D
nTH CELL VERIFIED
1803
PGM
1210

FIG. 25

	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

~~TABLE 1~~ FIG. 26

(typical values)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12v	$V_{CC}+\delta V$	V_{CC}	$V_{CC}-\delta V$
V_{CC}	5v	5v	5v	5v	5v
V_{PD}	V_{SS}	8v	8v	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20v	V_{SS}
unselected control gate	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
unselected bit line	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

V_{SS}=0V, V_{REF}=1.5V, δV=0.5V - 1V

~~TABLE 2~~ FIG. 27

Document1 - 1/10/08